

CLAIMS

What is claimed is:

- 1 1. A network processor comprising:
 - 2 a plurality of standard cells; and
 - 3 at least one field programmable gate array (FPGA) cell that can communicate
 - 4 with at least one of the standard cells, wherein the FPGA cell allows for customization of the
 - 5 network processor.

- 2 2. The network processor of claim 1, wherein the at least one FPGA cell can provide a specified function based upon field programming techniques to allow for customization of the network processor.

- 3 3. The network processor of claim 1 wherein the plurality of standard cells are utilized for common logic and the at least one FPGA cell is utilized for high risk logic.

- 4 4. A method for customizing a network processor; comprising the steps of:
 - 2 (a) providing at least one field programmable gate array (FPGA) cell within the network processor;
 - 3 (b) providing a custom logic file for the vendor of the network processor by a customer of the network processor; and
 - 4 (c) programming the at least one FPGA cell, the vendor based upon the custom logic bill to provide a customized network processor.

1 5. The method of claim 4 wherein step (b) further comprises (b1) providing a
2 verification module within the custom logic file.

1 6. The method of claim 4 which includes step (c) verifying the customized
2 network processor based upon the verification module.

1 7. A network processor comprising:
2 a plurality of standard cells, the plurality of standard cells comprising common logic;
3 a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and
4 at least one bus coupled to a portion of the standard cells and portion of the FPGA
5 cells, wherein each of the plurality of FPGA cells allows for customization of the network
6 processor.

1 8. The network processor of claim 7, wherein the plurality of cells each can
2 provide a specified function based upon field programming techniques to allow for
3 customization of the network processor.

1 9. The network processor of claim 7 wherein the at least one bus comprises a
2 processor local bus (PLB) and two on-chip peripheral buses (OPBs).

1 10. The network processor of claim 9 wherein the FPGA cells coupled to the PLB
2 comprise an accelerator function and a PLB master/slave function.

1 11. The network processor of claim 9 wherein the FPGA cells coupled to one of the
2 two OPBs are media interfaces.

1 12. The network processor of claim 9 wherein the FPGA cells coupled to the other
2 of the two OPBs are a GPIO preprocessor function and an OPB master/slave function.

1 13. A network processor comprising:
2 a plurality of standard cells, the plurality of standard cells comprising common logic;
3 a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and
4 a processor local bus (PLB) and two on-chip peripheral buses (OPBs) coupled to a portion of
5 the standard cells and portion of the FPGA cells, wherein the FPGA cells coupled to the
6 PLB comprise an accelerator function and a PLB master/slave function; wherein the FPGA
7 cells coupled to one of the two OPBs are media interfaces; wherein the FPGA cells coupled
8 to the other of the two OPBs are a GPIO preprocessor function and an OPB master/slave
9 function; wherein the plurality of cells each can provide a specified function based upon
10 field programming techniques to allow for customization of the network processor.